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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/560,634

12/13/2005

Cornelis Adrianus Mutsaers

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EXAMINER

RALEIGH, DONALD L

ART UNIT

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/560,634	<b>Applicant(s)</b> MUTSAERS, CORNELIS ADRIANUS	
	<b>Examiner</b> DONALD L. RALEIGH	<b>Art Unit</b> 2879	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 05 January 2009.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1 and 3-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 and 3-18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                 | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date: _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                        | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date: _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Response to Amendment***

The Amendment, filed on January 5, 2009 has been entered and acknowledged by the Examiner.

Claims 1, 3-18 are pending in the instant application.

### ***Claim Objections***

Claim 18 is objected to because of the following informalities: Claim 18 includes the limitation "planarisaiton material". For purposes of examination, it is assumed that applicant meant "planarisation material". Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

**Claims 1, 3, 7-11 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Fujiike et al (US Patent No. 7,014,521).**

**Regarding Claim 1**, Fujiike discloses in Figure 17A, a barrier laminate (color filter) including barrier (2, BM) and planarisation (3) materials for use with a device

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layer, comprising: a device layer (liquid crystal functional layers), and at least one discontinuous layer of a planarisation material (3) that is external to the device and corresponds to a stack including the device layer (liquid crystal functional layers), wherein the at least one discontinuous layer (color filter) is divided into unconnected areas distributed along a plane (Fig. 4) wherein the unconnected areas are separated by regions of a barrier material (2) and wherein the barrier material separating the unconnected areas is external to the device layer (Figure 17A) and is resistant to at least one of water and oxygen permeability such that the device layer is protected against physical degradation and/or oxidation due to environmental elements (although a separate protection layer is provided over the color filter and black matrix, the black matrix itself is a hard resin material (column 24, lines 22-24) and would resist, at least to some extent, water and oxygen permeability to the device layer.

**Regarding Claims 3, and 10-11,** Fujiike discloses a barrier laminate wherein said planarisation material is an organic material, an acrylate, or a polymeric material. Column 25 lines 16-24 disclose that the planarisation material (3) can have the same components as the ink used to form the colored layer of the filter. Column 18, line 20 discloses that the contents of the ink contains acrylic resin, which is an organic, polymeric acrylate.

**Regarding Claim 7,** Fujiike discloses in Figure 17B a barrier laminate further comprising at least one continuous layer of a barrier material (8).

**Regarding Claim 8**, Fujiike discloses in Figure 12E a barrier laminate wherein said discontinuous layer (color filter) is arranged between two continuous layers of a barrier material (8 and 1).

**Regarding Claim 9**, Fujiike discloses in Figures 17B, a barrier laminate (color filter) further comprising at least one continuous layer of a planarization material overcoat 8).

**Regarding Claim 17**, Fujiike discloses in Figures 6 and 12E a barrier laminate wherein the at least one discontinuous layer is positioned over active layers of an electronic device (liquid crystal device) and is, among layers of the laminate including planarisation material closest to the active layers (16) of said electronic device.

Figure 12E shows a barrier laminate on a color filter containing a discontinuous layer and figure 6 shows where that color filter laminate would be placed in conjunction with barrier laminate layer (8) adjacent to device layer (16).

**Claims 14-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Codama (US Patent No. 6,339,291).**

**Regarding Claim 14**, Codama discloses in Figures 2A to 2E, a method for the manufacture of a discontinuous layer in a barrier laminate for use with a device layer that includes two opposing electrodes(the first electrode (ITO)(26) is shown in the figures; the second electrode is not shown but disclosed in Column 8, lines 5-7),

comprising: depositing a continuous layer of a planarisation material (12)(Figure 2B); removing regions of said layer of a planarisation material (Figure 2C); and filling said regions with a barrier material (14) to form a barrier laminate layer (Figure 2E), wherein said regions are external to the device layer (11, ITO) and correspond to a stack including the device layer (11) such that the barrier material filling said regions is external to the device layer (the device layer is confined to the ITO region (11)) . (Column 6, lines 15-49 describes the process).

**Regarding Claim 15**, Codama discloses in Figures 2A to 2E, a method for the manufacture of a discontinuous layer in a barrier laminate for use with a device layer that includes two opposing electrodes (the first electrode (ITO)(26) is shown in the figures; the second electrode is not shown but disclosed in Column 8, lines 5-7)

comprising: depositing a patterned layer of a planarisation material (12)(the abstract discloses that layer (12) is placed and then patterned) whereby regions where no planarisation material is deposited are formed (see Figure 2C) and filling said regions with a barrier material (14)(see Figure 2E) to form a barrier laminate layer ((12a) and (14)) wherein said regions are external to the device layer (11)(shown in the figures) and correspond to a stack including the device layer (11)(the figures show that the discontinuous stacks of planarization material (12a) and barrier material (14) correspond in combination each to one device layer(11)) such that the barrier material (14) filling said regions is external to the device layer (11)(the barrier material encapsulates the device layer (11) and thus is external to it. See Figure 2F).

**Regarding Claim 16**, Codama discloses in Figures 2A to 2E, a method wherein said filling of said regions with a barrier material (14) is performed simultaneously as the deposition of a continuous layer of a barrier material (14) on said discontinuous layer (12) (Column 6, lines 15-49 describes the process).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiike (521) in view of Gotoh et al (US Patent No. 6,265,309).**

**Regarding Claim 4**, Fujiike fails to exemplify the limitation of said planarisation material is a combination of organic and inorganic materials.

Gotoh teaches a barrier laminate (Page 9, line 18, laminate) wherein said planarisation material (Column 9, line 19, smoothing film) is a combination of organic and inorganic materials (Column 9, lines 19-20).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to incorporate a planarisation material of both organic and inorganic materials, as taught by Gotoh, in the laminate of Fujiike, to realize the smoothing characteristics of the organic material with the moisture repellant qualities of the inorganic material.

**Claims 5, 12-13, are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiike (521) in view of Ghosh et al (US PG Pub. No. 2002/0003403).**

**Regarding Claims 5 and 12,** Fujiike fails to exemplify a barrier laminate wherein said barrier material is an inorganic material.

Ghosh(403) in Figure 3 teaches a barrier laminate (21,22,23, SiO<sub>2</sub>) wherein said barrier material is an inorganic material (Paragraph [0032], lines 26-30)(Line 30 teaches SiO<sub>2</sub> which is inorganic, to form a seal to prevent moisture from entering (Paragraph [0032], lines 19-23).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to incorporate the inorganic material, as taught by Ghosh(403), to form a seal to prevent moisture from entering .

**Regarding Claim 13,** Fujiike discloses a barrier laminate that is resistant to oxygen and water but fails to exemplify a barrier laminate wherein the barrier laminate is an oxygen and/or water impermeable film.

Ghosh(403), in Figure 3, teaches a barrier laminate (21,22,23, SiO<sub>2</sub>) wherein said barrier material is an oxygen and/or water impermeable film.(Paragraph [0032], lines 20-23) to form a seal to prevent moisture from entering.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to incorporate the oxygen and/or water impermeable film, as taught by Ghosh(403), to form a seal to prevent moisture from entering .



**Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiike (521) in view of Ghosh (US PG Pub. No. 2001/0052752).**

**Regarding Claim 6**, Fujiike fails to exemplify a barrier laminate wherein said regions of a barrier material forms a checked pattern.

Ghosh(752) teaches a barrier laminate wherein said regions (several regions including multiple devices are shown in Figure 5) of a barrier material forms a checked pattern (Figure 5 shows a checked pattern of a barrier material (21) exposing parts of the substrate)(Paragraph [0032], lines 17-19). Ghosh(752) provides this pattern as an obvious means of providing extended borders around the device layers to further protect them when the wafer is cut.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to incorporate the checkerboard pattern, as taught by Ghosh(752), in the laminate of Fujiike, to provide extended borders around the device layers to further protect them when the wafer is cut.

**Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiike (521) in view of Huzino et al (US Patent No. 4,983,469).**

**Regarding Claim 18**, Fujiike fails to exemplify the barrier laminate wherein the device layer includes pixels and wherein the barrier material separating the unconnected areas in the discontinuous layer of planarisation material is above or below the device layer in the stack.

Huzino teaches in Figure 8, the barrier laminate wherein the device layer (2 and 3 with the luminescent layer (1) between) includes pixels (one shown) and wherein the barrier material (9) separating the unconnected areas (4r,4b,4g) in the discontinuous layer of planarisation material is above the device layer in the stack to provide an improved contrast (Column 5, line 29).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine the structure of Huzino with the material of Fujiike, to provide a device with improved contrast.

### ***Response to Arguments***

Applicant's arguments with respect to claims 1 and 15 have been considered but are moot in view of the new ground(s) of rejection. The amendment of these claims raises new issues that require a new search and a new basis for rejection.

### ***Conclusion***

Applicant's amendment filed January 5, 2009 raises new issues that have necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

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shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DONALD L. RALEIGH whose telephone number is (571)270-3407. The examiner can normally be reached on Monday-Friday 7:30AM to 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh Patel can be reached on 571-272-2457. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For

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more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Peter J Macchiarolo/  
Primary Examiner, Art Unit 2879

/Donald L Raleigh/  
Examiner, Art Unit 2879